

REMARKS

The Abstract has been amended to be less than 150 words and to delete implied phrases, as requested by the Office Action. Claims 1-24 remain pending. Claims 1, 2, 7, 14-15, and 20 have been amended. Reconsideration and withdrawal of all outstanding rejections are respectfully requested in light of the foregoing amendments and the following remarks.

Claims 1-24 stand rejected under 35 USC 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Specifically, claims 1, 2, 7, 15, and 20 stand rejected for reciting "capable of" rather than a positive term, such as "for," as suggested by the Examiner. The claims have been amended to obviate the rejection, and withdrawal of the rejection is requested.

In addition, independent claims 1, 2, 7, 12, 15, and 20 stand rejected under 35 USC 112, second paragraph, as being indefinite. Specifically, the Office Action states that the respective preambles for these claims discuss, for example, a method for which the body of the claim does not provide structure for performing the method. Applicants respectfully disagrees with the conclusion that any of these claims is indefinite.

Claim 1 recites a method of performing a scan test on a semiconductor integrated circuit which has at least two blocks to be tested, each block for performing an active function. The method comprises isolating each of the blocks to be tested from other blocks and supplying a plurality of scan clocks, having different phases, to each of the blocks. There is nothing unclear or indefinite in what is being recited. The subject matter is unambiguous.

Claims 2 was specifically referenced in the Office Action as being rejected for reciting "a semiconductor integrated circuit for use in a scan test operation," which the Office Action asserts does not limit, in the body of the claim, the structure for performing the scan test. The preamble for this claim recites a semiconductor circuit which is to be tested with the elements and characteristics of the circuit recited in the body of the claim. There is nothing indefinite about the apparatus that is being tested or about what the apparatus comprises. Moreover, the Examiner's attention is directed to MPEP 211.02, where it explains that proper consideration should be given to "intended use" language in preambles, even if definitive structure for performing the use is not explicit in the body of the claim. MPRP 2111.02. For at least these reasons, reconsideration and withdrawal of the rejection are requested. Likewise, claims 7, 12, 15 and 20 are also not indefinite.

Claim 14 has been amended to correct the typographical error noticed by the Examiner to obviate the rejection. Other dependent claims 3-6, 13, 16-19, and 21-24 stand rejected as depending from a rejected base claim. While Applicants note that these claims should be subject to an objection rather than rejection, each claim should be allowable for at least the reasons stated above for the independent claims.

Claims 1-2, 7, 12-15, and 20 stand rejected under 35 USC 103(a) as being unpatentable over an article entitled, "Token Scan Architecture for Low Power Testing," by Huang et al ("Huang") in view of U.S. Patent No.6,018,815 to Baeg ("Baeg"). The rejection is traversed and reconsideration is requested.

The present invention relates to methods and circuit structures for performing a scan test on an integrated circuit. Specifically, the inventive method includes isolating at least two blocks for testing from other blocks in the integrated

circuit and supplying a plurality of scan clocks, each having different phases, to each of the at least two blocks.

Huang discloses a token scan circuit architecture for lowering the voltage power drops that have been known to cause malfunction while testing integrated circuits. Huang teaches use of multi-phase clocks as shown, for example in Fig. 10. Each set of multi-phase clocks are connected by one input to a group of testing blocks. See p. 665. Baeg discloses scan chips that can be configured in either a multiple scan chain or single scan chain mode where a multiplexer can provide multiple signals on multiple input lines to a series of blocks. Col. 5, lines 21-29. The multiple input lines of Baeg allow for multiple scan chain testing with reduced scan time over those in conventional circuits.

As acknowledged by the Examiner, Huang does not anticipate the present invention because Huang does not teach or suggest "isolating each of said at least two blocks to be tested exclusively from further blocks," as recited by claim 1. The Office Action attempts to cure this deficiency with the disclosure of Baeg which teaches a multiplexer 141 (Fig. 1) providing multiple clock signals on multiple outputs to blocks, allowing a multiple scan chain operation. This combination does not present a *prima facie* case of obviousness, however, because it is unclear how or why one of ordinary skill in the art would combine the teaching of Baeg of a multiplexer with multiple clock signal outputs with the multi-phase clocks, sharing a common output, as disclosed in Huang. MPEP 2143.

In addition, even if the multiplexer (141) of Baeg were combined with the multi-phase clocks of Huang, this combination would still not render the claimed combination obvious, as the multiphase clocks for each group of blocks share a common output line. Thus, even if the multiplexer 141 were added to the circuit, it

would still not be capable of "isolating each of said at least two blocks to be tested exclusively from further blocks," as in the present invention. For at least these reasons, reconsideration and withdrawal of the rejection of claim 1 is requested.

Each of the other independent claims recites a similar combination of elements that is not obvious in view of the references cited. Independent claim 2 recites a semiconductor integrated circuit comprising "an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and an input terminal for inputting a plurality of scan clocks [having different phases] to each of said at least two blocks." Independent claim 7 recites "an isolation unit for isolating each of said at least two blocks to be tested exclusively from further blocks; and a clock generator for generating a plurality of scan clocks [having different phases] based on a clock input from an exterior controllers each clock generator to be supplied to each of said at least two blocks." Independent claim 12 recites a tester comprising "a circuit that isolates at least two blocks of an integrated circuit to be tested exclusively from further blocks of said circuit and supplies a plurality of scan clocks to each of said at least two blocks, said plurality of scan clocks each having a phase different from each other." And finally, independent claim 20 recites a circuit comprising "means for isolating each of said at least two block means to be tested exclusively from further block means; and means for generating a plurality of scan clocks [having different phases] based on a clock input from an exterior controller to be supplied to each of said at least two block means." Claims 13-14 depend from claim 12.

For all of the reasons given above, the combination of references, whether considered alone or in combination, does not render claims 1, 2, 7, 12-15 and 20 obvious. Reconsideration and withdrawal of the outstanding rejections is requested.

In view of the above amendment, applicant believes the pending application is in condition for allowance.

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Respectfully submitted,

By 

Thomas J. D'Amico

Registration No.: 28,371

Megan S. Woodworth

Registration No.: 53,655

DICKSTEIN SHAPIRO LLP

1825 Eye Street, N.W.

Washington, DC 20006-5403

(202) 420-2200

Attorneys for Applicant